REMARKS

The Official Action dated May 12, 2006 has been received and its contents carefully noted. In view of thereof, claims 1, 11 and 16 have been amended in order to better define that which Applicant regards as the invention. As previously, claims 1-20 are presently pending in the instant application.

Turning now to the Official Action particularly page 2 thereof, claim 16 has been objected to as including a minor informality. In this regard, as can be seen from the foregoing amendments, claim 16 has been amended to correct that informality noted by the Examiner. Accordingly, we respectfully submitted that the pending claim 16 is now in proper formal condition for allowance.

With reference to paragraph 4 of the Office Action, claims 1-3, 7, 9, 11-13, 17 and 19 have been rejected under 35 U.S.C. § 102(e) as being anticipated by U.S. Patent Publication 2002/01844712 to Hatae et al. This rejection is respectfully traversed in that Hatae et al neither discloses nor suggests that which is presently set forth by Applicants claimed invention.

As can be seen from the foregoing amendments, each of the independent claims 1 and 11 have been amended in order to better define that which Applicant regards as the invention. Specifically, independent claim 1 and similarly independent claim 11 recites a semiconductor integrated circuit comprising a central possessing unit, a main memory control unit for controlling a main memory, an I/O channel control unit for controlling a peripheral device, a first bus for connecting the central processing unit, main memory control unit and I/O channel control unit to each other, a local memory for storing information, a second bus for connecting the local memory to the central processing unit, an access control means for accessing the local memory in response to a request from the outside, and a third bus for

directly connecting the local memory to the access control means. It is respectfully submitted that these features are neither disclosed in nor suggested by the prior art of record.

Particularly, Applicants claimed invention encompasses essentially two embodiments wherein each embodiment includes a local memory. In the first embodiment illustrated in Figure 1, the local memory has two ports with the local memory being directly connected to a central processing unit by a second bus. Therefore, it is possible to transmit data between the local memory and the central processing unit at very high speeds. The high speed data transmission takes place independently of other circuits and can be carried out without being influenced by other circuits. The local memory is also directly connected to an access control means or access controller by a third bus. Therefore, as noted above, it is possible to transmit data between the local memory and the access control means at very high speeds. The high speed data transmission takes place independently of other circuits and can be carried out without being influenced by the other circuits.

Similarly, in a second embodiment illustrated in Figure 2, a local memory, an arbitration means and a selection circuit are set forth. Based on the arbitration results of the arbitration means, the central processing unit is connected to the local memory by way of the selection circuit or the access control means is connected to the local memory by way of the selection circuit. In doing so, the local memory, central processing unit and access control means have independent buses and are connected to the selection circuit independently. Better stated, one-to-one connection is established between the local memory and selection circuit, one-to-one connection is established between the central processing unit and selection circuit and one-to-one connection is established between the access control means and selection circuit. In doing so, the central processing unit can directly access the local memory, and the access control means can directly access the local memory. Clearly, the

prior art of record neither discloses or suggests these features.

Particularly, with respect to the teachings of Hatae, this reference utilizes a two port buffer RAM 9 to establish the access to an external device by way of the data transfer controller 5. In Hatae, however, the data is transmitted between the buffer not in a central processing unit by way of a SIMD unit 3. In Hatae, the central processing unit is not directly connected to the buffer RAM 9 as is specifically recited by Applicants' claimed invention. The roles of the central processing unit and buffer RAM of Hatae are also different from that of the present invention. Particularly, the central processing unit is designed to handle the expanded image data, and the buffer RAM 9 is designed to store the compressed image data. Thus, direct connection between the central processing unit and buffer RAM 9 is clearly not of concern with respect to the teachings of Hatae. Consequently, it is respectfully submitted that Hatae cannot achieve the high speed accessing from the central processing unit to the memory data as is this with the present invention.

Accordingly, it is respectfully submitted that Applicants claimed to invention as set forth in each of independent claims 1 and 11 as well as those claims which depend therefrom are neither anticipated by or rendered obvious in view of the teachings of Hatae et al.

With reference to paragraph 6 of the Office Action, claims 4-6, 8, 14-16 and 18 have been rejected as being unpatentable over Hatae et al and U.S. Patent No. 4,523,272 issued to Fukunaga et al. This rejection is respectful traversed in that the patent to Fukunaga et al does nothing to overcome the aforementioned shortcomings associated with the teachings Hatae et al.

Particularly, in reviewing the teachings of Fukunaga, this reference discloses a device to select one of a plurality of buses for connecting between a memory and a plurality of processors. As shown in Figure 1 of Fukunaga and as appreciated by the Examiner,

processors are connected to the memory by selected single bus. The selection of a certain bus in Fukunaga does not correspond to the selection by the selection circuit of Claim 4 because all of the processors are connected to the memory in Fukunaga, whereas the single processor is connected to the memory as recited in claim 4 of Applicants claimed invention. In accordance with the present invention, the local memory, central processing unit and access control means are connected to the selection circuit by way of the respective independent buses. More importantly, Fukunaga is directed to very old technology which teaches simple arbitration of a common bus. Clearly, Fukunaga neither discloses nor remotely suggests the use of selection circuit similar to that of Applicants claimed invention. Accordingly, it is respectfully submitted that Applicant's claimed invention as set forth in Claims 4-6, 8, 14-16, and 18 clearly distinguishes over the combination proposed by the Examiner and is in proper condition for allowance.

With reference now to paragraph 7 of the Office Action, claims 10 and 20 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Hatae et al in view of Fukunaga et al and further in view of U.S. Patent Publication No. 2004/0049293 issued to Hadwiger et al. This rejection is likewise respectfully traversed in that Patent Publication to Hadwiger et al. clearly fails to overcome the aforementioned shortcomings associated with Hatae et al. when taken alone or in view of the teachings of Fukunaga.

In reviewing Hadwiger et al, it is noted that this reference disclosed arbitration units 314, 315 and 316. However, the arbitration units of Hadwiger are significantly different from that of Fukunaga. The arbitration units 315, 315 and 316 are used to connect selected buses to each other in Hadwiger. Whereas a plurality of processors are connected to the selected one of the buses in Fukunaga. The arbitration unit of Fukunaga allows one of the processors to use that particular bus. Consequently, it is respectfully submitted that the modification of

the combination of Hatae in view of Fukunaga with the teachings of Hadwiger and particularly the modification of the arbitration units of Fukunaga in view of the teachings of Hadwiger are not well founded. Moreover, it is respectfully submitted that even if such combination is made, the device set forth in each of independent claims 1 and 11 is not achieved. Accordingly, it is respectfully submitted that Applicants claimed invention as set forth in dependent claims 10 and 20 likewise distinguishes over the combination proposed by the Examiner and is in proper condition for allowance.

Therefore, its respectfully requested that the objections and rejections of record be reconsidered and withdrawn by the Examiner, that claims 1-20 be allowed and that the application be passed to issue.

Should the Examiner believe a conference would be of benefit in expediting the prosecution of the instant application, he is hereby invited to telephone counsel to arrange such a conference.

Respectfully submitted,

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